PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Charles E. Larson

Serial No.: 10/667,003

Filed: September 19, 2003

For: METHODS RELATING TO FORMING INTERCONNECTS AND RESULTING ASSEMBLIES

Confirmation No.: 6648

Examiner: J. Maldonado

Group Art Unit: 2823

Attorney Docket No.: 2269-5682US (02-1370)

Notice of Allowance Mailed:

February 1, 2005

Express Mail Mailing Label No.:	EL 994849172 US
Date of Deposit with USPS:	April 29, 2005
Person making Deposit:	Steve Wong

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Examiner indicates:

The prior art of record teach away from securing a first and second semiconductor substrates having an interposing dielectric element, forming an interconnect void, and injecting a flowable conductive material into said void. (¶ 5, Notice of Allowability).

Applicant concurs with the reasons as stated by the Examiner insofar as they comprise a summary, and are exemplary and not limiting. However, the independent claims as allowed include other and different language than that specified by the Examiner, and the allowed dependent claims include other and further features and elements. Accordingly, the scope of the claims must be determined from the literal language of each as a whole, as well as equivalents thereof.

Respectfully submitted,

Bretton L. Crockett
Registration No. 44,632
Attorney for Applicant
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: April 29, 2005
BLC/nj:dn
Document in ProLaw